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| EXAMINER | |
|---|---|
| MORTELL, JOHN F | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/562,458 | BREDERLOW ET AL. | |
| | Examiner | Art Unit | |
| | JOHN F. MORTELL | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of the Application*

1. This application is proceeding pursuant to the amendment filed August 14, 2009. Claims 12-31 are pending in the application. The applicants have amended claim 12 to correct minor typographical errors. The applicants previously cancelled claims 1-11.

### *Response to Arguments*

2. The applicants' arguments, see "REMARKS," filed August 14, 2009, with respect to claims 12-31 have been fully considered and are persuasive. The Non-Final Rejection of May 14, 2009, has been withdrawn.

### *Claim Rejections - 35 USC § 102*

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.

4. Claim 12-20 and 22-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Noto (US 5,731,691).

Regarding claim 12, Noto discloses:

> an electronic component operable with an AC voltage (col. 4, lines 30-33; FIG. 1), the electric component comprising:
>
> at least one input (FIG. 1: 1);
>
> at least one output (FIG. 1: 9);
>
> and a pair of functionally identical electronic sub-components, wherein the

> functionally identical electronic sub-components are connected in parallel (col. 4, lines 15-28; FIG. 1: 8a, 8b);
>
> wherein the at least one input of the electronic component is connected to a respective input of the two functionally identical electronic sub-components (FIG. 1: 1 and input to 8a);
>
> wherein the at least one output of the electronic component is connected to a respective output of the two functionally identical electronic sub-components (FIG. 1: 9 and output of 8a);
>
> wherein the electronic component is configured such that at the at least one output only one output signal of a first sub-component of the pair of functionally identical electronic sub-components can be picked up during a first half-wave of an AC voltage, whereas only one output signal of the second sub-component of the pair of functionally identical electronic sub-components can be picked up during a second half-wave of the AC voltage (col. 4, lines 15-40; FIG. 1).

Regarding claim 13, Noto discloses the electronic component of claim 12, which includes a pair of functionally identical electronic sub-components, and the inclusion of a plurality of pairs of functionally identical electronic sub-components is merely redundancy that does not provide a new or unexpected result and therefore, does not distinguish the component from the component recited in claim 12.

Regarding claim 14, Noto further discloses an electronic component wherein at least one pair of functionally identical electronic sub-components comprises one of logic-gates, inverters, and flip-flops. (col. 4, lines 15-28; FIG. 1: 8a, 8b; Noto discloses diodes in parallel, and a diode is a semiconductor device that changes state from off to on when the input voltage increases above the bias voltage, which is typically 0.6-0.7 V. A device that changes state in response to a change in voltage is a logic gate.)

Regarding claim 15, Noto discloses a component wherein the electronic component comprises a coil. (col. 4, lines 4-5; FIG. 1: 6)

Regarding claim 16, Noto discloses an electronic component further comprising a voltage limiter, which limits the AC voltage lying across an electronic sub-component of the pair of functionally identical electronic sub-components. (col. 4, lines 15-28; FIG. 1: 8)

Regarding claim 17, Noto further discloses an electronic component wherein the electronic sub-components of a pair of functionally identical electronic sub-components comprises a switch. (col. 4, lines 15-28; FIG. 1: 8a, 8b; Noto discloses diodes in parallel, and a diode is a semiconductor device that changes state from off to on when the input voltage increases above the bias voltage, which is typically 0.6-0.7 V. A device that changes state from off to on in response to a change in voltage is a switch.)

Regarding claim 18, Noto discloses an electronic component wherein the electronic component is configured within an ID tag. (col. 1, lines 12-13; col. 3, lines 23-28)

Regarding claim 19, Noto discloses an electronic component wherein the ID tag comprises a memory for storing information. (col. 1, lines 12-13; col. 3, lines 23-28)

Regarding claim 20, Noto discloses an electronic component wherein the ID tag comprises an encoder for coding information. (col. 4, lines 41-46)

Regarding claim 22, Noto discloses:

> a read device (col. 3, lines 23-25);
>
> an ID tag with an electric component (col. 1, lines 12-13; col. 3, lines 23-28) comprising:
>
> an electronic arrangement (col. 3, lines 21-23; FIG. 1) comprising:
>
> a first sub-component with an input and an output (col. 4, lines 15-28; FIG. 1: 8a);
>
> a second sub-component with an input and an output, wherein the first and the second sub-components are connected in parallel (col. 4, lines 15-28;

FIG. 1: 8b);

an AC signal received by the inputs of the first and second sub-components, the AC signal having a first half-wave and a second half-wave (col. 4, lines 30-33; Noto discloses an AC electromotive force, and an AC electromotive force inherently consists of a first half-wave and a second half-wave.);

means for providing an output from only the first sub-component during the first half-wave (col. 4, lines 15-28; FIG. 1); or

means for providing an output from only the second sub-component during the second half-wave (col. 4, lines 15-28; FIG. 1);

wherein the ID tag and read device are configured to communicate with each other without contact (col. 3, lines 23-26; FIG. 1).

Regarding claim 23, Noto discloses an electronic arrangement wherein the first and second sub-components are functionally substantially similar. (col. 4, lines 15-28; FIG. 1: 8a, 8b)

Regarding claim 24, Noto discloses the electronic arrangement of claim 23, which includes a pair of functionally identical electronic sub-components, and the inclusion of a plurality of pairs of functionally identical electronic sub-components is merely redundancy that does not provide a new or unexpected result and therefore, does not distinguish the arrangement from the arrangement recited in claim 23.

Regarding claim 25, Noto discloses an electronic arrangement wherein at least one pair of functionally identical electronic sub-components comprises one of logic-gates, inverters and flip-flops. (col. 4, lines 15-28; FIG. 1: 8a, 8b; Noto discloses diodes in parallel, and a diode is a semiconductor device that changes state from off to on when the input voltage increases above the bias voltage, which is typically 0.6-0.7 V. A device that changes state in response to a change in voltage is a logic gate.)

Regarding claim 26, Noto discloses an electronic arrangement wherein the electronic component is a coil. (col. 4, lines 4-5; FIG. 1: 6)

Regarding claim 27, Noto discloses an electronic arrangement wherein the electronic component further comprises a voltage limiter, which limits the AC voltage lying across an electronic sub-component of the pair of functionally identical electronic sub-components. (col. 4, lines 15-28; FIG. 1: 8)

Regarding claim 28, Noto discloses an electronic arrangement wherein the electronic sub-component comprises a switch. (col. 4, lines 15-28; FIG. 1: 8a, 8b; Noto discloses diodes in parallel, and a diode is a semiconductor device that changes state from off to on when the input voltage increases above the bias voltage, which is typically 0.6-0.7 V. A device that changes state from off to on in response to a change in voltage is a switch.)

Regarding claim 29, Noto discloses an electronic arrangement wherein the ID tag comprises a memory for storing information. (col. 1, lines 12-13; col. 3, lines 23-28)

Regarding claim 30, Noto discloses an electronic arrangement wherein the ID tag comprises an encoder for coding information. (col. 4, lines 41-46)

### *Claim Rejections - 35 USC § 103*

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.

6. Claims 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noto in view of Baude et al. (US PG Pub. 2004/0119504 A1) and further in view of Bayron et al. (US 5,769,051).

Regarding claim 21, Noto does not disclose an electronic component wherein the encoder is configured such that it can be used for pulse-coding and pulse-coding.

Baude, in the same field of endeavor, teaches an RFID tag with an electronic component that comprises an encoder configured such that it can be used for pulse-coding for the benefit of outputting data to a reader unit. ([0057], [0060]; FIG. 11: 72, 76)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the RFID tag with an electronic component that comprises an encoder configured such that it can be used for pulse-coding, as taught by Baude, with the electronic component disclosed by the above combination because it would enable the component to output data to a reader unit.

The above combination of Noto and Baude does not teach an electronic component wherein the encoder is configured such that it can be used for time-coding.

Bayron, in the same field of endeavor, teaches a passive transponder wherein the encoder is configured such that it can be used for time-coding for the benefit of enabling a keychain unit to operate as a passive transponder for interfacing with an engine controller. (col. 2, lines 33-34, 64-65; col. 6, lines 57-64; FIG. 7: 96)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the passive transponder wherein the encoder is configured such that it can be used for time-coding, as taught by Bayron, with the electronic component disclosed by the above combination because it would enable the component to operate as a passive transponder for interfacing with an engine controller.

Regarding claim 31, Noto does not disclose an electronic arrangement wherein the

encoder is configured such that it can be used for pulse-coding.

Baude, in the same field of endeavor, teaches an RFID tag with an electronic component that comprises an encoder configured such that it can be used for pulse-coding for the benefit of outputting data to a reader unit. ([0057], [0060]; FIG. 11: 72, 76)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the RFID tag with an electronic component that comprises an encoder configured such that it can be used for pulse-coding, as taught by Baude, with the electronic arrangement disclosed by the above combination because it would enable the arrangement to output data to a reader unit.

The above combination of Noto and Baude does not teach an electronic arrangement wherein the encoder is configured such that it can be used for time-coding.

Bayron, in the same field of endeavor, teaches a passive transponder wherein the encoder is configured such that it can be used for time-coding for the benefit of enabling a keychain unit to operate as a passive transponder for interfacing with an engine controller. (col. 2, lines 33-34, 64-65; col. 6, lines 57-64; FIG. 7: 96)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the passive transponder wherein the encoder is configured such that it can be used for time-coding, as taught by Bayron, with the electronic arrangement disclosed by the above combination because it would enable the arrangement operate as a passive transponder for interfacing with an engine controller.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN F. MORTELL whose telephone number is (571)270-1873. The examiner can normally be reached on IFP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel J. Wu can be reached on (571)272-2964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JM/

/Daniel Wu/
Supervisory Patent Examiner, Art Unit 2612